Mentor Graphics

"Verification of Electronic Design and Systems using System Verilog training Program

Only for 2016 Passing Out Batch Students

About the Program

"Verification of Electronic Design and Systems using System Verilog" for students. The course will be for 6 weeks and it will include projects and extensive labs using Mentor Tools. This is a free program for candidates selected through Mentor Graphics all India selection Program.

"Verification of Electronic Design and Systems using System Verilog" is intended to be an introductory course for a fresh graduate interested in pursuing a career in the semiconductor and Electric System Design industry. The course will be taught using System Verilog Hardware Verification Language constructs and OVM Technology.

Duration : Starting From June 1, 2015 to July 17, 2015 (Mon to Sat)

Some of the Key Modules of the Program are

1) Introduction to Logic Design & Verification (Block Level & System Level)
2) Introduction to System Verilog as a Verification Language
3) Introduction to System Verilog Open Verification Methodology
4) Concepts of Verification Management & Coverage using Questa Verification Environment.

(The program will include extensive labs using labs using Mentor Tools and some projects)

Eligibility

1) 2016 Passing Out Batch
2) Students pursuing B.Tech in Electronics, Electrical, Computer Engineering
3) CGPA Min. 7 and above
4) Completed 6^{th} Semester
5) M.Tech Students – The Candidate Should not be employed in any company at the time of training

(Students who have completed their B.Tech / M.Tech need not apply)

Selection Criteria

A total of 30 students will be selected for this program. Shortlisted candidates will be notified by May 1st Week. The selection process will be conducted at Mentor Graphics office (Bangalore/ Noida). Mentor Graphics selction will be final. The selected candidates will have to make his/ her own stay and travel arrangements.

PROGRAM HAS NO FEE

Interested Students Need to register at http://www.mentor.com/systemverilog-training

All the Best!

With Warm Regards

Dr. Ajay S Rana